AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

Claims 1-20. **(Cancelled)**

Claim 21. **(Cancelled)**

Claim 22. **(Cancelled)**

Claim 23. **(Currently Amended)** The charge pump circuit of claim ~~21~~29, where the FETs are PFETs.

Claim 24. **(Currently Amended)** The charge pump circuit of claim ~~21~~29, where the first pump stage of each cascade is coupled to ~~the~~ a power supply voltage.

Claim 25. **(Currently Amended)** The charge pump circuit of claim ~~21~~29, where each pump cascade is coupled to the output node by a coupling diode.

Claim 26. **(Previously Presented)** The charge pump circuit of claim 25, where the coupling diode is a diode connected FET having a gate oxide of the second oxide thickness.

Claim 27. **(Cancelled)**

Claim 28. **(Currently Amended)** The charge pump of claim ~~22~~29, where the first and second non-overlapping clock signals are generated from a system clock signal and the charge pump stages pump charge to the output node in response to both a rising edge and a falling edge of ~~the~~ a system clock signal.

Claim 29. **(Currently Amended)** A charge pump power supply for a DRAM, comprising a charge pump circuit comprising a first and a second pump cascade

coupled in parallel to an output node, each pump cascade having a plurality of pump stages coupled in series, the output node receiving charge pumped by the first and the second pump cascades and providing an output supply voltage that is greater in magnitude than a power supply voltage; each pump stage having a FET configured as a diode and a FET configured as a capacitor, the FETs of a first pump stage of each pump cascade having a first oxide thickness and the FETs of a last pump stage of each pump cascade having a second oxide thickness, the second oxide thickness being greater than the first oxide thickness; each (2n)th pump stage of the first pump cascade is coupled to a first non-overlapping clock signal and each (2n+1)th pump stage of the first pump cascade is coupled to a non-overlapping second clock signal, n being an integer greater than or equal to zero; each (2n)th pump stage of the second pump cascade is coupled to the second non-overlapping clock signal and each (2n +1)th pump stage of the second pump cascade is coupled to the first non-overlapping clock signal, n being an integer greater than or equal to zero; and ~~The charge pump circuit of claim 27, where the first and second clock signals are generated from~~

a ~~non~~ non-overlapping clock signal generator for supplying the first and second non-overlapping clock signals, comprising: a system clock input node; a clock input stage; a latch coupled to the clock input stage having intermediate latch outputs and complementary latch outputs; clock output driving stages coupled to the complementary latch outputs and having ~~non~~ non-overlapping clock signal outputs; and an equalization stage coupled between the clock output driving stages and receiving as inputs the intermediate latch outputs.

Claim 30. **(Cancelled)**

Claim 31. **(Currently Amended)** A charge pump power supply for use in a DRAM comprising a charge pump cascade having a plurality of pump stages coupled in series with each pump stage having a FET configured as a diode and a FET configured as a capacitor; the FETs of a first of the pump stages having a first oxide thickness and the FETs of a last of the pump stages having a second oxide thickness, the second oxide thickness being greater than the first oxide thickness; the first pump stage coupled to a power supply voltage; a~~The charge pump cascade of claim 30, wherein~~ (2n)th pump stage of the pump cascade is coupled to receive a first non-overlapping clock signal and

(2n+1)th pump stage of the pump cascade is coupled to receive a second non-overlapping clock signal, n being an integer greater than or equal to zero.; and

a non-overlapping clock signal generator for supplying the first and second non-overlapping clock signals, comprising a system clock input node; a clock input stage; a latch coupled to the clock input stage having intermediate latch outputs and complementary latch outputs; clock output driving stages coupled to the complementary latch outputs and having non-overlapping clock signal outputs; and an equalization stage coupled between the clock output driving stages and receiving as inputs the intermediate latch outputs.

Claim 32. **(Currently Amended)** The charge pump circuit of claim 3031, wherein the FETs are PFETs.

Claim 33. **(Currently Amended)** The charge pump cascade of claim 3031, wherein the pump cascade is coupled to the output node by a diode connected FET having a gate oxide of the second oxide thickness.

Claim 34. **(Cancelled)**

Claim 35. **(Currently Amended)** A method for providing a charge pump ~~circuit~~ power supply for a DRAM comprising ~~the~~ steps of:

coupling first and second pump cascades in parallel to an output node, each pump cascade having a plurality of pump stages coupled in series; ~~receiving at said output node charge pumped by the first and the second pump cascades to generate a supply voltage thereat that is greater in magnitude than a power supply voltage; and~~

~~constructing~~ providing each pump stage ~~from~~ with a FET configured as a diode and a FET configured as a capacitor, the FETs of ~~the~~ a first pump stage of each pump cascade having a first oxide thickness and the FETs of ~~the~~ a last pump stage of each pump cascade having a second oxide thickness, the second oxide thickness being greater than the first oxide thickness.;

coupling each 2(n)th pump stage of the first pump cascade and each 2(n+1)th pump stage of the second pump cascade to a first non-overlapping clock signal and each

2(n+1)th pump stage of the first pump cascade and each 2(n)th pump stage of the second pump cascade to a second non-overlapping clock signal; and

providing a non-overlapping clock signal generator for supplying the first and second non-overlapping clock signals by coupling a system clock input node to a clock input stage, coupling a latch having intermediate latch outputs and complementary latch outputs to the clock input stage; coupling an equalization stage to the intermediate latch outputs and between clock output driving stages; and coupling the clock output driving stages to the complementary latch outputs to generate the non-overlapping clock signals.